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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,013	CHU ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-84* is/are pending in the application.

4a) Of the above claim(s) *45-57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11,21,33,58,59,70,71,82 and 83* is/are rejected.

7)☒ Claim(s) *2-10,12-20,22-32,34-44,60-69,72-81 and 84* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-44 and 58-84 in the response filed 10 September 2004 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 11, 21 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The final element of each of the above-mentioned claims is "a Si cap layer on top of said top $Si_{1-m}Ge_m$ buffer layer that is under tensile strain". It is not clear if the cap layer is under tensile strain, or if the buffer layer is under tensile strain, and where in the specification such a limitation is recited.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 58 and 82 are rejected under 35 U.S.C. 102(e) as being unpatentable over Kubo et al..

As to claim 1, Kubo et al., Figure 18, and paragraph [0187] discloses a semiconductor layer structure

comprising a relaxed p-doped $Si_{1-x}Ge_x$ layer, embodied as a p-type graded SiGe layer (102), a bottom $Si_{1-z}Ge_z$ buffer layer, embodied as a p-type relaxed SiGe buffer layer (103), on top of said relaxed $Si_{1-x}Ge_x$ layer, a tensile strained Si quantum well layer (104), and a top $Si_{1-m}Ge_m$ buffer layer, embodied as a relaxed SiGe layer (105), on top of said tensile-strained Si quantum well layer. Kubo et al. further discloses in paragraph [0201] that it is known in the art that a conventional Si-MISFET would have a Si cap layer on top of said top $Si_{1-m}Ge_m$ buffer layer.

As to claim 58, Kubo et al., paragraphs [0187] and [0192] disclose an insulating gate dielectric (106) located on top of said Si cap layer, a gate electrode (107) located on top of said insulating gate dielectric, n-type source and drain contact regions located on either side of said gate electrode, which extend from the surface of the structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer (103), and trench isolation regions (Figure 22, element 123) on either side of the source and drain contact regions, which penetrate into said relaxed $Si_{1-x}Ge_x$ layer.

As to claim 82, Kubo et al., paragraph [0187] discloses that the insulating gate dielectric (106) is a nitride, and that the gate electrode is an Al-Cu alloy, paragraph [0089].

Claim 11, 59 and 83 are rejected under 35 U.S.C. 102(e) as being unpatentable over Kubo et al.. As to claim 11, Kubo et al., Figure 18, and paragraph [0187] discloses a semiconductor layer structure comprising a relaxed p-doped $Si_{1-x}Ge_x$ layer, embodied as a p-type graded SiGe layer (102), a bottom $Si_{1-z}Ge_z$ buffer layer, embodied as a p-type relaxed SiGe buffer layer (103), on top of said relaxed $Si_{1-x}Ge_x$ layer, a tensile strained Si quantum well layer (104), and a top $Si_{1-m}Ge_m$ buffer layer, embodied as a relaxed SiGe layer (105), on top of said tensile-strained Si quantum well layer. Since the relaxed p-doped $Si_{1-x}Ge_x$ layer is embodied as a p-type graded SiGe layer (102), this layer is within the scope of being two separate graded layers, one with molar composition $Si_{1-x}Ge_x$ and the other, which would serve as an interposer layer, with molar composition $Si_{1-y}Ge_y$, where $x \neq y$. Kubo et al. further discloses in paragraph [0201] that it is known in the art that a conventional Si-MISFET would have a Si cap layer on top of said top $Si_{1-m}Ge_m$ buffer layer.

As to claim 59, Kubo et al., paragraphs [0187] and [0192] disclose an insulating gate dielectric (106) located on top of said Si cap layer, a gate electrode (107) located on top of said insulating gate

dielectric, n-type source and drain contact regions located on either side of said gate electrode, which extend from the surface of the structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer (103), and trench isolation regions (Figure 22, element 123) on either side of the source and drain contact regions, which penetrate into said relaxed $Si_{1-x}Ge_x$ layer.

As to claim 83, Kubo et al., paragraph [0187] discloses that the insulating gate dielectric (106) is a nitride, and that the gate electrode is an Al-Cu alloy, paragraph [0089].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al., Figure 18 in view of Kubo et al., Figure 16. As to claim 21, Kubo et al., Figure 18, and paragraph [0187] discloses a semiconductor layer structure comprising a relaxed p-doped $Si_{1-x}Ge_x$ layer, embodied as a p-type graded SiGe layer (102), a bottom $Si_{1-z}Ge_z$ buffer layer, embodied as a p-type relaxed SiGe buffer layer (103), on top of said relaxed $Si_{1-x}Ge_x$ layer, a tensile strained Si quantum well layer (104), and a top $Si_{1-m}Ge_m$ buffer layer, embodied as a relaxed SiGe layer (105), on top of said tensile-strained Si quantum well layer. Kubo et al. further discloses in paragraph [0201] that it is known in the art that a conventional Si-MISFET would have a Si cap layer on top of said top $Si_{1-m}Ge_m$ buffer layer. Kubo et al., Figure 18, does not disclose expressly a relaxed n-doped $Si_{1-x}Ge_x$ layer, or a compressive-strained $Si_{1-v}Ge_v$ quantum well layer formed between $Si_{1-z}Ge_z$ buffer layers. Kubo et al., Figure 16, and paragraphs [0168] and [0169], discloses a compressively-strained SiGe quantum well channel layer (82) formed on an n-type Si substrate (80). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form a compressively-strained SiGe channel layer in place of the tensile-strained Si quantum well layer of Figure 18, and to dope the relaxed $Si_{1-x}Ge_x$ layer as n-type. The motivation for doing so would have

been to increase the speed of the device by utilizing light holes that are produced by the degeneracy slitting of the valence band, as in paragraphs [0023] and [0024]. Therefore, it would have been obvious to combine the compressive layer of Figure 16 with the device of Figure 18 of Kubo et al. to obtain the invention as specified in claim 21.

As to claim 70, Kubo et al., paragraphs [0187] and [0192] disclose an insulating gate dielectric (106) located on top of said Si cap layer, a gate electrode (107) located on top of said insulating gate dielectric, n-type source and drain contact regions located on either side of said gate electrode, which extend from the surface of the structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer (103), and trench isolation regions (Figure 22, element 123) on either side of the source and drain contact regions, which penetrate into said relaxed $Si_{1-x}Ge_x$ layer.

Claims 33 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al., Figure 18 in view of Kubo et al., Figure 16. As to claim 33, Kubo et al., Figure 18, and paragraph [0187] discloses a semiconductor layer structure comprising a relaxed p-doped $Si_{1-x}Ge_x$ layer, embodied as a p-type graded SiGe layer (102), a bottom $Si_{1-z}Ge_z$ buffer layer, embodied as a p-type relaxed SiGe buffer layer (103), on top of said relaxed $Si_{1-x}Ge_x$ layer, a tensile strained Si quantum well layer (104), and a top $Si_{1-m}Ge_m$ buffer layer, embodied as a relaxed SiGe layer (105), on top of said tensile-strained Si quantum well layer. Since the relaxed p-doped $Si_{1-x}Ge_x$ layer is embodied as a p-type graded SiGe layer (102), this layer is within the scope of being two separate graded layers, one with molar composition $Si_{1-x}Ge_x$ and the other, which would serve as an interposer layer, with molar composition $Si_{1-y}Ge_y$, where $x \neq y$. Kubo et al. further discloses in paragraph [0201] that it is known in the art that a conventional Si-MISFET would have a Si cap layer on top of said top $Si_{1-m}Ge_m$ buffer layer. Kubo et al., Figure 18, does not disclose expressly a relaxed n-doped $Si_{1-x}Ge_x$ layer, or a compressive-strained $Si_{1-v}Ge_v$ quantum well layer formed between $Si_{1-z}Ge_z$ buffer layers. Kubo et al., Figure 16, and paragraphs [0168] and [0169], discloses a compressively-strained SiGe quantum well channel layer (82) formed on an n-type Si substrate (80). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form a compressively-strained SiGe channel layer in place of the tensile-strained Si quantum well layer of Figure 18, and to dope the relaxed $Si_{1-x}Ge_x$ layer as n-type. The motivation for doing so would have

been to increase the speed of the device by utilizing light holes that are produced by the degeneracy slitting of the valence band, as in paragraphs [0023] and [0024]. Therefore, it would have been obvious to combine the compressive layer of Figure 16 with the device of Figure 18 of Kubo et al. to obtain the invention as specified in claim 33.

As to claim 71, Kubo et al., paragraphs [0187] and [0192] disclose an insulating gate dielectric (106) located on top of said Si cap layer, a gate electrode (107) located on top of said insulating gate dielectric, n-type source and drain contact regions located on either side of said gate electrode, which extend from the surface of the structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer (103), and trench isolation regions (Figure 22, element 123) on either side of the source and drain contact regions, which penetrate into said relaxed $Si_{1-x}Ge_x$ layer.

Allowable Subject Matter

Claims 2-5 and 64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Kubo et al., nor any other prior art discloses the $Si_{1-z}Ge_z$ buffer layers to be undoped. The corresponding buffer layers of Kubo et al. are p-doped.

Claims 6-10, 60, 61, 66 and 67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The bottom $Si_{1-z}Ge_z$ buffer layer and the top $Si_{1-m}Ge_m$ buffer layer of Kubo et al. are uniformly p-doped. No prior art discloses the claimed structure with partially doped SiGe buffer layers.

Claims 12-15, 19, 20, 65, 68, 69 and 84 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Kubo et al., nor any other prior art discloses the $Si_{1-z}Ge_z$ buffer layers to be undoped. The corresponding buffer layers of Kubo et al. are p-doped.

Claims 16-18, 62 and 63 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and

any intervening claims. The bottom $Si_{1-z}Ge_z$ buffer layer and the top $Si_{1-m}Ge_m$ buffer layer of Kubo et al. are uniformly p-doped. No prior art discloses the claimed structure with partially doped SiGe buffer layers.

Claims 22-26 and 76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Kubo et al., nor any other prior art discloses the $Si_{1-z}Ge_z$ buffer layers to be undoped. The corresponding buffer layers of Kubo et al. are p-doped.

Claims 27-32, 72, 73, 78 and 79 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The bottom $Si_{1-z}Ge_z$ buffer layer and the top $Si_{1-m}Ge_m$ buffer layer of Kubo et al. are uniformly p-doped. No prior art discloses the claimed structure with partially doped SiGe buffer layers.

Claims 34-38 and 77 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Kubo et al., nor any other prior art discloses the $Si_{1-z}Ge_z$ buffer layers to be undoped. The corresponding buffer layers of Kubo et al. are p-doped.

Claims 39-44, 74, 75, 80 and 81 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The bottom $Si_{1-z}Ge_z$ buffer layer and the top $Si_{1-m}Ge_m$ buffer layer of Kubo et al. are uniformly p-doped. No prior art discloses the claimed structure with partially doped SiGe buffer layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
December 6, 2004

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